

REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-8 and 10 are active in this application, Claims 1 and 7 having been amended by way of the present Amendment and Claims 9 and 11-18 previously withdrawn from consideration as being directed to a non-elected invention.

In the outstanding Office Action Claims 1, 4, 5, 7 and 10 were rejected under 35 USC §102(b) as being anticipated by Tokura et al (6,015,737), Claims 1, 6 and 10 were rejected under 35 USC §102(b) as being anticipated by Baba et al (5,126,807), Claim 2 was rejected under 35 USC §103(a) as being unpatentable over Tokura et al in view of Suzuki et al (JP-2000269487) and Claims 3 and 8 were objected to as being dependent upon a rejected base clam, but otherwise allowable if rewritten in independent form.

In light of the outstanding grounds for rejection, Claim 1 has been amended to clarify that the first and second gate electrodes which are separate from each other are formed on a gate insulating film and opposed to the facing side surfaces of a trench. Support for the changes to Claim 1 is found in the exemplary embodiment of Figure 2. Claim 8 has been amended to clarify that the connection of the first and second gate electrodes occurs at a different portion of the device, i.e., at a part thereof inside the trench above a non-inversion region beneath the trench. Support for the amendment to Claim 8 is found in the disclosure of Figures 10-11 and the corresponding discussion at page 15, lines 12-27. No new matter has been added.

Tokura et al. discloses a MOSFET having n⁻-type epitaxial layer (drain) 2, p-type base layer 16, n⁺-type source layer 4, U-groove 50, gate oxide film 8, and gate electrode 9, as shown in FIG. 22, etc. P-type base layer 16 is formed on n⁻-type epitaxial layer 2 and n⁺-type source layer 4 is formed on p-type base layer 16. U-groove 50 is formed in p-type base

layer 16. Gate electrode 9 is formed on the inside surface of U-groove 50 through gate oxide film 8.

Amended Claim 1 differs from Tokura et al. in the several respects. The first and second gate electrodes of amended Claim 1 are formed on the gate insulating film and opposed to the facing side surfaces of a trench. The first and second electrodes are separate from each other. According to the outstanding Official Action, Tokura et al. discloses first (part of part 9 facing left) and second (part of part 9 facing right) gate electrodes 9, and that they are connected at a part (part of part 9 facing down) thereof inside trench 50. Amended Claim 1 and Tokura et al. may be similar to each other in that gate electrodes are formed on the facing side surfaces of a trench. Although the first and second gate electrodes of amended Claim 1, each of which is formed on one of the facing side surfaces, are separate from each other, the gate electrodes of Tokura et al. are continuously formed as one piece on the facing side surfaces. Thus, Tokura et al. do not disclose any equivalent for the first and second gate electrode which are formed on the facing side surfaces of the trench and separate from each other.

In view of this distinction, it is believed to be clear that Tokura et al. do not disclose the claimed first and second gate electrode of amended Claim 1, which are formed on the gate insulating film and opposed to the facing side surfaces of the trench, and separate from each other. Therefore, it is respectfully submitted that the subject matter of amended Claim 1 is not anticipated by Tokura et al. and that the outstanding rejection of Claims 1, 4, 5, 7 and 10 under 35 USC §102(b) as being anticipated by Tokura et al. has been overcome.

Turning now to the outstanding rejection of Claims 1, 6 and 10 under 35 U.S.C. 102(b) as being anticipated by Baba et al., Baba et al. disclose a MOS transistor having drain region 3, channel region 5, source region 7, trench 23, gate insulation film 9, and gate electrode 17, as shown in FIG. 5, etc. Channel region 5 is formed on drain region 3 and

source region 7 is formed on channel region 5. Trench 23 is formed across drain region 3, channel region 5 and source region 7. Gate electrode 17 is formed on the inside surfaces of trench 23 thorough gate insulation film 9.

In contrast, according to amended Claim 1, the depth of a trench is shorter than the depth of the deepest bottom portion of a second semiconductor region. The outstanding Official Action finds that Baba et al. disclose that the depth of trench 23 is shorter than the depth of the deepest bottom portion of channel region 5. Amended claim 1 and Baba et al. may be similar to each other in that trench is formed across the surface of a source region to the source region and a base region. Although the depth of the trench is shorter than the depth of the deepest bottom portion of the second semiconductor region in amended claim 1, the depth of trench 23 is deeper than the depth of the deepest bottom portion of channel region 5 in Baba et al. Thus, Baba et al. do not disclose the trench whose depth is shorter than the depth of the deepest bottom portion of the second semiconductor region.

From the above discussion, it is respectfully submitted that Baba et al. do not disclose the trench of amended Claim 1 whose depth is shorter than the depth of the deepest bottom portion of the second semiconductor region. Therefore, it is respectfully submitted that the subject matter of amended Claim 1 is not anticipated by Baba et al. and that the outstanding rejection of Claims 1, 6 and 10 under 35 USC §102(b) as being anticipated by Baba et al. has been overcome.

The remaining cited references have also been considered but are believed to be no more pertinent to patentability of Claim 1 than the references above discussed.

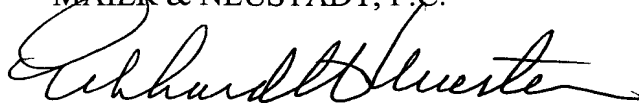
Consequently, in view of the present amendment and in light of the above discussion,

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the pending active claims are believed to be in condition for formal allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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